Please amend the present application as follows:

Specification

The following is a marked-up version of the specification with the language that is underlined ("___") being added and the language that contains strikethrough ("—") being deleted:

Page 3, lines 19 through 21.

Two parity symbols are required to locate and correct a full error while only one parity symbol is required to correct an erasure error. While not all storage systems implementing an ECC are capable of detecting erasures, the ability to detect and correct erasures can substantially improve the capability of a given coding scheme.

Page 6, lines 16 through 29.

Interrupt systems and methods of the present invention will now be explained in greater detail with reference to the drawings. In FIG. 1, an embodiment of a system 5 of the present invention includes a host 10, such as a personal computer or other computer system that relies upon access to memory. The host 10 may also be an external testing system used during manufacturing of a storage device. Alternatively, the host 10 may be an internal testing system within a storage device for executing self-tests and requesting the execution of a Verify procedure, such as the continuous verification procedure as described in co-pending U.S. Patent Application Serial Number 10/092,111 (HP Docket No. 10018461-1), which is hereby incorporated by reference in its entirety into the present disclosure. The host 10 interacts with a data storage device 14 via a storage device controller 12. The host 10 is connected to the

storage device controller 12 along line 16. Line 16 may include any type of serial or parallel path for electrical communication between the host 10 and storage device controller 12.

Page 19, lines 15 through 21.

Also, in cooperation with co-pending application 10/092,111 (HP Docket No. 10018461-1), counters can be used to figure out how often an error is detected in a defective location. Oftentimes in memory devices, errors may not show up on every pass, but only occasionally. A benefit of using this type of counter in the Verify procedure of the co-pending application 10/092,111 (HP Docket No. 10018461-1) is to detect the memory locations that do not reveal "soft" or random errors that are not consistently repeatable.